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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/052,277
Filing Date: January 17, 2002
Appellant(s): JENSEN, JENSEN HARTRUNG

Michael Ure (Reg. No. 33,089)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 05/29/2007 and a supplemental appeal brief filed 02/25/2008 appealing from the Office action mailed 09/26/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US Patent	5,987,614	Mitchell et al.	11-1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8, 10-13 and 15-19 are rejected under 35 U.S.C. 102(b) as being anticipated 20 by Mitchell et al. [US 5,987,614 A; hereinafter Mitchell].

Referring to claim 1, Mitchell discloses a system (i.e., distributed power management system; See col. 1, lines 5-10) comprising:

- a plurality of components (i.e., Subsystem 1 .... Subsystem n in Fig. 3) each having a bus interface (i.e., Clock Gate Logic 53 and Bus I/F 54 in Fig. 3),

- a bus structure (i.e., Data 71, Address 72, Bus Controls & Status 73, and Bus Clock 74 in Fig. 3) that is configured to facilitate communications among said plurality of components (See col. 7, lines 39-44), and

- an activity detector (i.e., Central PMU 42 of Fig. 1 and 3; See col. 6, lines 47-50) that is configured to detect an initiation (i.e., detecting an occurrence of particular system resource activity; See col. 1, lines 32-44) of a data-transfer operation (i.e., bus cycle for data transfer; See col. 7, lines 39-54) and to provide therefrom an enabling signal (i.e., ON/DOZE/SLEEP/SUSPEND signal as discussed in Fig. 1 embodiment, and power down/up signal on Power Down 75 of Fig. 3 embodiment; See col. 1, line 51 through col. 2, line 6) that is communicated to bus interfaces (i.e., said Clock Gate Logic and Bus I/F; See Fig. 3) of a plurality of said components (i.e., said Subsystem 1, ... Subsystem n; See col. 6, lines 50-58), wherein

  - said bus interface (i.e., said Clock Gate Logic and Bus I/F) is configured to be enabled to receive data from said bus structure (i.e., said Data, Address, Bus Controls & Status, and Bus Clock) as part of said data-transfer operation (i.e., said bus cycle for data transfer) upon receipt of said enabling signal from said activity detector (See col. 7, line 55 through col. 8, line 3 and col. 9, lines 54-61).

Referring to claim 2, Mitchell teaches

- said activity detector (i.e., Central PMU 42 of Fig. 3) is configured to detect a completion of said data-transfer operation (See col. 2, lines 25-31 ; i.e., detecting a completion of the particular bus cycle using a predetermined idle time), and terminates said enabling signal (i.e., ON~DOZE--,SLEEP-,SUSPEND) based on said completion of said data-transfer operation (i.e., based on said predetermined idle time; See col. 2, lines 31-44), and
- said bus interface (i.e., Clock Gate Logic 53 and Bus I/F 54 in Fig. 3) is configured to be disabled from receiving data from said bus structure upon termination of said enabling signal (See col. 1, line 51 through col. 2, line 6; in fact, SUSPEND signal disables receiving data from bus structure).

Referring to claim 3, Mitchell teaches

- said enabling signal (i.e., ONIDOZEISLEEP/SUSPEND signal and power down/up signal on Power Down 75 of Fig. 3) includes a gated clock signal (i.e., said power down/up signal on said Power Down is directly input to Clock Gate Logic 53 in Fig. 3; See col. 9, lines 54-65).

Referring to claim 4, Mitchell teaches

- said bus interface (i.e., Clock Gate Logic 53 and Bus I/F 54 in Fig. 3) includes a plurality of clocked devices (i.e., Clock Gate Logic 63, Master I/F Block 86, and Slave I/F Block 88 in Fig. 5) that are clocked based on said enabling signal (i.e., said Clock Gate Logic, said Master I/F Block, and said Slave I/F Block are being clocked based on enabling status of ON/DOZE/SLEEP/SUSPEND signal and power down/up signal on Power Down 75 of Fig. 3).

Referring to claim 5, Mitchell teaches said activity detector (i.e., Central PMU 42 of in Fig. 3) includes:

- a set-reset device (i.e., Activity Monitors 21 of Fig. 1) that is set (i.e., operating to trigger a particular predetermined action) upon detection of said initiation of said data-transfer operation (i.e., upon the occurrence of one or more pre-identified addresses or address ranges on address bus; See col. 1, lines 44-50), and
- a delay device (i.e., Activity Timers 23 of Fig. 1), operably coupled to said set-reset device (i.e., said Activity Monitors and Activity Timers are operable coupled; See col. 2, lines 42-44), that is configured to provide said enabling signal (i.e., ON/DOZE/SLEEP/SUSPEND signal and power down/up signal on Power Down 75 of Fig. 3) synchronous with a system clock (i.e., said Central PMU is synchronized with Bus Clock bclk 74 in Fig. 3) that is common to said bus structure (i.e., Data 71, Address 72, Bus Controls & Status 73, and Bus Clock 74 in Fig. 3; See col. 7, lines 38-43), based on whether said set-reset device is set (See col. 1, lines 31-50).

Referring to claim 6, Mitchell teaches

- said set-reset device (i.e., Activity Monitors 21 of Fig. 1) is reset (i.e., no triggering operation based on no activity being monitored on Address Bus 26 and Bus Controls 27 in Fig. 1) upon detection of a completion of said data-transfer operation (i.e., detecting of bus idle; See col. 2, lines 25-40).

Referring to claim 7, Mitchell teaches

- a bus controller (i.e., Central Bus Interface 43, in fact, Bus Arbiter Logic 130 in Fig. 3) that is configured to establish a communications path (i.e., communication path between Master device and Slave device; See col. 14, lines 58-65 and Fig 11) between an initiating component (i.e., any Subsystem requesting resources as said Master device on a target Subsystem in Fig. 3) of said plurality of components (i.e., Subsystem 1, ... Subsystem n in Fig. 3) and a target component (e.g., Subsystem 1 51 as said Slave device in Fig. 3) of said plurality of components,
  - wherein said activity detector (i.e., Central PMU 42 of Fig. 3) provides said enabling signal (i.e., ON/DOZE/SLEEP/SUSPEND signal and power down/up signal on Power Down 75 of Fig. 3; See col. 1, line 51 through col. 2, line 6) within a time duration consumed by said bus controller to establish said

communications path (i.e., the time duration for establishing communication path from said Master device to said Slave device by way of arbitration is longer than the time duration for providing the enabling signal by way of monitoring bus activity because the communication path should be established for the communication between said Master device and said Slave device after the activity detector generates the enabling signal, which clearly anticipates said activity detector providing said enabling signal within a time duration consumed by said bus controller to establish said communications path; See col. 15, lines 5-15).

Referring to claim 8, Mitchell teaches said bus controller (i.e., Central Bus Interface 43 of Fig. 3) including

- one or more devices (i.e., Clock Div. Notify 44, Clock Freq. Control 45, Latency Timer 46, and Bus Arbiter Logic 130 in Fig. 3) that operate in dependence upon said enabling signal (i.e., said Central Bus Interface is operating in dependence upon Bus Clock(f2) from Central PMU 42 via host bus 41 in Fig. 3; See col. 3, lines 3-13).

Referring to claim 10, Mitchell discloses a method of reducing power consumption in a system (i.e., distributed power management system; See col. 3, lines 66-67) comprising

- a plurality of components (i.e., Subsystem 1 .... Subsystem n in Fig. 3) each having a bus interface (i.e., Clock Gate Logic 53 and Bus I/F 54 in Fig. 3), that are configured to communicate via a bus structure (i.e., Data 71, Address 72, Bus Controls & Status 73, and Bus Clock 74 in Fig. 3; See col. 7, lines 39-44), comprising:
  - detecting an initiation (i.e., detecting an occurrence of particular system resource activity) of a data-transfer operation (i.e., bus cycle for data transfer; See col. 7, lines 39-54) by a component of said plurality of components (See col. 1, lines 32- 44),
  - communicating an enabling signal (i.e., ON/DOZE/SLEEP/SUSPEND signal and power down/up signal on Power Down 75 of Fig. 3; See col. 1, line 51 through col. 2, line 6) to more than one other components of said plurality of components (i.e., said Subsystem 1 .... Subsystem n; See col. 6, lines 50-58), and
  - enabling a bus interface (i.e., Clock Gate Logic 53 and Bus I/F 54 in Fig. 3) at each of said more than one other components (i.e., said Subsystem 1 and Subsystem n) to receive data signals as part of said data-transfer operation (i.e., said bus cycle for data transfer), based on said enabling signal (i.e., said Clock Gate Logic, said Master I/F Block, and said Slave I/F Block are being clocked based on enabling status of ON/DOZE/SLEEP/SUSPEND signal and power down/up signal on Power Down 75 of Fig. 3).

Referring to claim 11, Mitchell teaches

- detecting a completion of said bus activity (See col. 2, lines 25-31; i.e., detecting a completion of the particular bus cycle using a predetermined idle time), and
- disabling said bus interface (i.e., Clock Gate Logic 53 and Bus I/F 54 in Fig. 3) at each of said more than one other components (i.e., Subsystem 1 .... Subsystem n in Fig. 3), based on said completion of said bus activity (See col. 1, line 51 through col. 2, line 6; in fact, SUSPEND signal disables receiving data from bus structure).

Referring to claim 12, Mitchell teaches

- synchronizing said enabling signal (i.e., ON/DOZE/SLEEP/SUSPEND signal and power down/up signal on Power Down 75 of Fig. 3) to a system clock (i.e., Central PMU 42 is synchronized with Bus Clock bclk 74 in Fig. 3) that is common to said bus structure (i.e., Data 71, Address 72, Bus Controls & Status 73, and Bus Clock 74 in Fig. 3; See col. 7, lines 38-43), based on whether said set-reset device is set (See col. 1, lines 31-50).

Referring to claim 13, Mitchell teaches

- establishing a communicatio.ns path (i.e., communication path between Master device and Slave device; See col. 14, lines 58-65 and Fig 11) between said component that initiated said bus activity (i.e., any Subsystem requesting resources as said Master device on a target Subsystem in Fig. 3) and a target component (e.g., Subsystem 1 51 as said Slave device in Fig. 3) of said more than one other components (i.e., Subsystem 1 ... Subsystem n in Fig. 3), and
- enabling said bus interface (i.e., Clock Gate Logic 53 and Bus I/F 54 in Fig. 3) at said target component within a time duration required to establish said communications path (i.e., the time duration for establishing communication path from said Master device to said Slave device by way of arbitration is longer than the time duration for providing the enabling signal by way of monitoring bus activity because the communication path should be established for the communication between said Master device and said Slave device after the activity detector generates the enabling signal, which clearly anticipates said activity detector providing said enabling signal within a time duration consumed by said bus controller to establish said communications path; See col. 15, lines 5-15).

Referring to claim 15, Mitchell discloses an electronic circuit (i.e., distributed power management system; See col. 1, lines 5-10, Figs. 1 and 3) comprising:

- a plurality of initiators (i.e., Subsystems 1…n in Fig. 3) that are configured to selectively initiate data-transfer operations (i.e., requesting resources which are included in target; See col. 7, lines 47-54) via a bus structure (i.e., Data 71, Address 72, Bus controls & status 73, Bus clock 74, Power down 75 and Central bus interface 43 in Fig. 3),
- an activity detector (i.e., Address Comparison Logic 92 and Clock Control Gate Logic 53 in Fig. 4) that is configured to detect an initiation of a data-transfer operation from any of said plurality of initiators (See col. 7, lines 43-46 and 55-57; i.e., detecting a particular bus cycle), and to generate therefrom an enabling signal (i.e., gbclk 57, e.g., gbclk 57a and gbclk 57n, in Fig. 3),
- a plurality of targets (i.e., Subsystem 1 ....Subsystem n in Fig. 3) that are configured to process said data-transfer operations (i.e., providing requested resources; See col. 7, lines 55-61), each of said plurality of targets (e.g., Subsystems in Fig. 3) including
  - an interface (i.e., core logic 52, e.g., core logic 1 52a, in Fig. 3) for receiving said data-transfer operations, wherein
    - said interface (i.e., said core logic) of each of said plurality of targets is configured to receive data of said data-transfer operations in dependence upon said enabling signal from said activity detector (See col. 7, line 59 through col. 8, line 3).

Referring to claim 16, Mitchell teaches

• said plurality of initiators (i.e., Subsystem 1 ....Subsystem n in Fig. 3) are configured to effect said data-transfer operations at a system clock speed (i.e., bus clock bclk in Fig. 8; in fact, all the Subsystems are operating under the system bus clock bclk 74 in Fig. 3), and
• said interface (i.e., core logic 52, e.g., core logic 1 52a, in Fig. 3) of each of said plurality of targets is configured to operate at said system clock speed (i.e., bclk speed in Fig. 8) only when said activity detector (i.e., Address Comparison Logic 92 and Clock Control Gate Logic 53 in Fig. 4) provides said enabling signal (i.e., gbclk 57 in Fig. 3; See col. 13, line 40 through col. 14, line 13).

Referring to claim 17, Mitchell teaches said enabling signal (i.e., gbclk 57, e.g., gbclk 57a and gbclk 57n, in Fig. 3) includes
• a clocking signal that operates at said system clock speed (i.e., a gated clock signal gbclk 67 from control gate logic 63 in Fig. 7).

Referring to claim 18, Mitchell teaches said activity detector is configured
• to detect a completion of said data-transfer operations (See col. 8, lines 3-5; i.e., detecting a completion of the particular bus cycle), and
• to terminate said generation of said enabling signal (e.g., disabling gbclk 57a of Fig. 3) based on a completion of said data-transfer operations (See col. 8, lines 5-8).

Referring to claim 19, Mitchell teaches
• a bus controller (i.e., Address Decode Logic 91 and Address Comparison Logic 92 in Fig. 4) that is configured to establish a communications path (See col. 18, lines 3-25 and Fig 16) between an initiator of said plurality of initiators (i.e., any one of Subsystems requesting resources on a target Subsystem in Fig. 3) and a target (e.g., Subsystem 1 51 in Fig. 3) of said plurality of targets,
- wherein said activity detector (i.e., Address Comparison Logic 92 and Clock Control Gate Logic 53 in Fig. 4) is configured to generate said enabling signal (i.e., gbclk 57, e.g., gbclk 57a and gbclk 57n, in Fig. 3) within a time duration required by said bus controller to establish said communications path (i.e., the time duration for establishing communication path from CPU to Subsystem 1 is longer than the time duration for providing the enabling signal because the communication path should be established after the activity detector generates the enabling signal, which clearly anticipates said activity detector is configured to generate said enabling signal within a time duration required by said bus controller to establish said communications path; See col. 7, line 38 through col. 8, line 3 and Fig. 3).

(10) Response to Argument

(i) Regarding Appellant's argument that Mitchell does not teach "***an enabling signal*** *(singular) that is communicated to* ***bus interfaces*** *(plural) of a plurality of components. Rather, Mitchell teaches bus interfaces of each of plurality of components* ***each providing its own separate enabling signal.*** *That enabling signal* ***(sell-n)*** *is communicated* ***only to its own bus interface*** *(i.e. clock gate logic 53a-n)*" (page 8 of the Brief):

First, it is noted that Appellant's assertion that the enabling signal being the **sell-n signal** in Mitchell is not correct, because the Rejection clearly stated the enabling signal being the **ON/DOZE/SLEEP/SUSPEND signal** and **power down/up signal on Power Down 75** (col. 1 line 51 to col. 2 line 6, Fig. 1 and Fig. 3).

a) Mitchell's Fig. 3 embodiment:

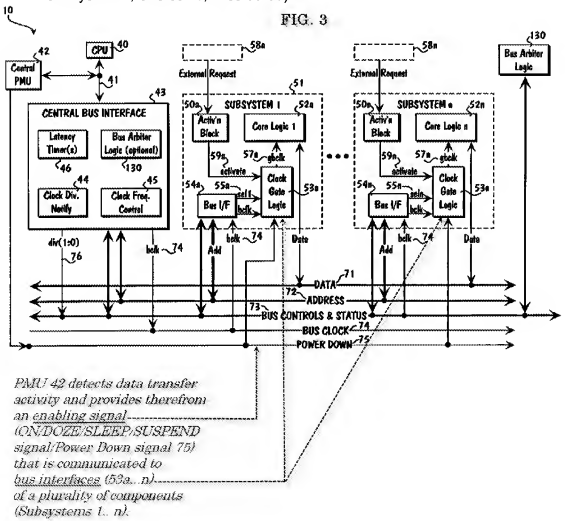
Mitchell teaches an inventive power management system **(Fig. 3)**, and states that the system may optionally, but advantageously, **also include** a **centralized power management unit 42** (in **Fig. 1) of conventional type** (col. 6 lines 44-58). The detail description of the conventional centralized power management unit 42 is being shown and disclosed in Mitchell's Fig. 1 and col. 1 line 32 et seq.:

> "The centralized power management unit (PMU) passively watches activity on the bus concerning other system resource units. The occurrence of one or more pre-identified addresses or address ranges on address bus 26 is recognized by the activity monitor, which in turn operates to trigger a particular predetermined action, such as to alter the operating state or mode of one or more system devices to affect a change in the power consumption state of the system" (col. 1 lines 42-50).
>
> "In one conventional power management system, five operating states are provided: ON, DOZE, SLEEP, SUSPEND, and OFF. These names are not uniformly standardized, but each of the DOZE, SLEEP, and SUSPEND modes represents intermediate power consumption states between fully ON and fully OFF" (col. 1 lines 51-56).
>
> "With further reference to FIG. 1, the power state block 24 controls the system power management state and interfaces to the clock control logic 25. Clock control logic block 25 receives a clock input signal (clock_ in) at a first clock frequency (f1) and controls the state of the output bus clock. Clock control 25 may pass the clock_ in signal through, may slow the clock to a lower frequency (f2), or may stop the bus clock for the entire system during certain low power consumption power management states" (col. 3 lines 3-11).

Therefore, with the inclusion of the conventional centralized power management (PMU 42, Fig. 1) in the system of Fig. 3, the PMU 42 provides the system with additional functions as discussed above. And thus, Mitchell clearly teaches:

> • an activity detector (**PMU 42**) that is configured to detect an initiation of a data-transfer operation (**detecting an occurrence of data transfer activity by the activity monitor 21**) and to provide therefrom an enabling signal (**ON/DOZE/SLEEP/SUSPEND signal, or Power Down signal 75**) that is communicated to bus interfaces (i.e., said Clock Gate Logic and Bus I/F; See Fig. 3) of a plurality of said components (i.e., said Subsystem 1, ... Subsystem n; See col. 6, lines 50-58):

FIG. 3

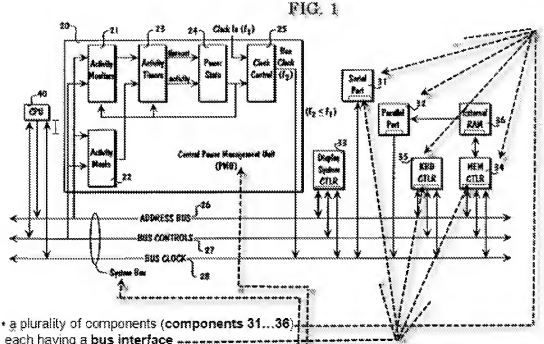


Thus, Fig. 3 embodiment discloses an enabling signal that is communicated to bus interfaces of a plurality of components, and Appellant's argument on this point is not persuasive.

b) Mitchell's Fig. 1 embodiment:

It is further noted that while **Fig. 3** embodiment was discussed in detail in the Rejection for the convenience of Applicant because Fig. 3 provides a more detail view of the system, conventional **Fig. 1** embodiment alone, in fact, also teaches all the claimed invention:

FIG. 1



- a plurality of components (**components 31...36**), each having a **bus interface** (each component must include an interface to transmit/receive signals from others),

- a bus structure (**System bus 26, 27,...**) that is configured to facilitate communications among said plurality of components, and

- an activity detector (**PMU**) that is configured to detect an initiation of a data-transfer operation (**detecting an occurrence of data transfer activity by the activity monitor 21**) and to provide therefrom an enabling signal (**ON/DOZE/SLEEP/SUSPEND signal**) that is communicated to bus interfaces of a plurality of said components, wherein

- said bus interface is configured to be enabled (turned to **ON**) to receive data from said bus structure (**Data/Address/Controls/Clock**) as part of said data-transfer operation upon receipt of said enabling signal from said activity detector (col. 1 lines 32-56).

Therefore, either one of Fig. 1 or Fig. 3 embodiments discloses an enabling signal that is communicated to bus interfaces of a plurality of components, and thus Appellant's argument on this point is not persuasive.

(ii) Regarding Appellant's argument of claim 10 that Mitchell does not teach "*communicating an **enabling signal** to **more than one** other components of the plurality of components, and **enabling a bus interface at each** of the more than one other component... Rather, Mitchell teaches communicating an enabling signal only within a single component, and enabling the bus interface at that component only*" (page 9 of the Brief):

As discussed above, the enabling signal (ON/DOZE/SLEEP/SUSPEND signal/ Power Down 75) is communicated to multiple interfaces (53a…n) of multiple components (Subsystems 1…n) (**more than one components**) to enable the interfaces at those components. And thus, Appellant's argument on this point is not persuasive.

(iii) Regarding Appellant's argument of claim 15 that Mitchell does not teach "*an activity detector that is configured to detect an initiation of a data transfer operation from any of the plurality of initiators, and to generate therefrom **an enabling signal**,...wherein the interface of **each of the plurality of targets** is configured to receive data of the data-transfer operations in dependence upon the upon **the enabling signal** from the activity detector. Rather, Mitchell teaches each of a plurality of targets being configured to receive data in dependence upon its own enabling signal*" (page 9 of the Brief):

a) First, it is noted that Mitchell discloses all the limitations in claim 15, as the claim recites similar limitations as discussed above with respect to Figs. 1 and 3 embodiments, i.e. activity detector (**PMU 42**) detects data transfer activity from any of the initiators (**subsystems 1…n**) and generates therefrom an enabling signal (**ON/DOZE/SLEEP/SUSPEND signal/Power Down signal 75**).

b) Furthermore, another interpretation of the Mitchell reference also anticipates claim 15. Mitchell teaches that besides the external enabling signal (**ON/DOZE/SLEEP/SUSPEND signal/Power Down signal 75**), there is also an internal enabling signal (**gbclk signal**) within each subsystem. This interpretation as well anticipates claim 15 as detailed above in the Rejection.

Appellant further argues that "*wherein the interface of* ***each of the plurality of targets*** *is configured to receive data of the data-transfer operations in dependence upon* ***the enabling signal*** *from the activity detector. Rather, Mitchell teaches each of a plurality of targets being configured to receive data in dependence upon its* ***own enabling signal***". It is noted to Appellant that the enable signal can be of any kinds, e.g. own enabling signal, external enabling signal, etc. The claim language does not require that the enable signal must be an external enabling signal (i.e. not the subsystem's own enabling signal). The features upon which Appellant relies (i.e., Appellant's enable signal is not the target's own enable signal) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Therefore, Appellant's argument on this point is not persuasive.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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